Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An image data reducing device for image data composed of a plurality of components, the image data having data corresponding one-to-one to each pixel with respect to a given component among the plurality of components, and having data common to a plurality of pixels with respect to the other components, the image data reducing device, comprising:

a reduced image data generating circuit that receives input image ~~data that is input so that~~ data, the input image data being configured such that data of each component of the plurality of components has a series relationship with each other, ~~and that generates~~the reduced image data generating circuit generating reduced image data ~~after being reduced~~ so as to output the reduced image ~~data after being reduced;~~ data; and

an output control signal generating circuit that generates an output control signal that controls whether each component of the input image data is output or not based on a decimation pattern ~~of input component~~ that is determined depending on a format of the input image data and a reduction ratio, the reduced image data generating circuit including a switching circuit that controls a presence of output for each component of the input image data being input in series based on the output control signal.

2. (Currently Amended) The image data reducing device according to Claim 1,

the output control signal generating circuit further comprising:

a counting circuit that counts input of the given component, ~~and that resets~~ the counting circuit resetting a counted value in a case where the counted value reaches a reciprocal number of the reduction ratio so as to restart counting, based on information about the format of the input image data and information about the reduction ratio; and

a decimation pattern information storing unit that stores ~~unit storing~~ decimation pattern information set in correlation with the counted value of the given component, the output control signal being generated based on the counted value of the given component and the decimation pattern information.

3. (Currently Amended) An image data reducing device reducing YUV image data, comprising:

a reduced image data generating circuit that receives input YUV image ~~data that is input so that~~data, the input YUV image data being configured such that data of each component of YUV has a series relationship with each other, ~~and that generates~~the reduced image data generating circuit generating reduced YUV image data ~~after being reduced~~ so as to output the reduced YUV image ~~data after reduced;~~data; and

an output control signal generating circuit that generates ~~circuit generating~~ an output control signal that controls whether each component of ~~YUV~~ of the input YUV image data is output or not based on a decimation pattern of input component that is determined depending on a format of the input YUV image data and a reduction ratio,

the reduced image data generating circuit including a switching circuit that controls a presence of output for each component of the input YUV image data being input in series based on the output control ~~signal;~~signal,

the output control signal generating circuit including:

a counting circuit that counts input of Y component, ~~and that resets~~the counting circuit resetting counted value in the case where the counted value of Y component reaches a reciprocal number of the reduction ratio so as to restart counting, based on information about the format of the input YUV image data and information about the reduction ratio; and

a decimation pattern information storing unit that stores decimation pattern information set in correlation with the counted value ~~of the~~ of Y component; and

the output control signal being generated based on the counted value of the Y component and the decimation pattern information.

4. (Currently Amended) The image data reducing device according to ~~Claim 1,~~Claim 3,

the reduced image data generating circuit including a common data storing unit that retains the other components or UV component that is input and has data common to a plurality of pixels, the reduced image data generating circuit generating reduced image data by using data stored in the common data storing unit based on the output control signal; and

the output control signal generating circuit that determines whether reduced image data is generated by using data stored in the common data storing unit or not, based on the counted value of the Y component and the decimation pattern information, the output control signal generating circuit generating the output control signal directing to generate reduced image data by using data stored in the common data storing unit in a case where generating of reduced image data by using data stored in the common data storing unit is determined.

5. (Previously Presented) The image data reducing device according to Claim 1,

input data being received as parallel data with bandwidth equal to a bit number of each component; and

the reduced image data generating circuit controlling a presence of output for each bit of the parallel data base on the output control signal.

6. (Previously Presented) The image data reducing device according to Claim 1,

a reduction ratio setting register setting reduction ratio information being included; and

reduction ratio being determined based on the reduction ratio information set in the reduction ratio setting register.

7. (Previously Presented) The image data reducing device according to Claim 1,

a format information setting register setting format information of input image data being included; and

a format of input image data being determined based on the format information set in the format information setting register.

8. (Previously Presented) A micro computer comprising the image data reducing device according to Claim 1.

9. (Previously Presented) An electronic apparatus, comprising:

the micro computer according to Claim 8;

an input device that inputs data to be processed by the micro computer; and

LCD output device that displays data that has been processed by the micro computer.